WHAT IS CLAIMED IS:

1. A gateway card that is connected to an information processor and that receives and transmits data between different networks, the information processor having a normal power mode and a power saving mode, the gateway card comprising:

a switching unit that connects a memory with either the information processor or the gateway card; and

a switch control unit that controls the switching unit to connect the memory to the information processor when the information processor is in the normal power mode, and controls the switching unit to connect the memory to the gateway card when the normal power mode of the information processor is changed to the power saving mode.

2. The gateway card according to claim 1, wherein

the switch control unit controls the switching unit to connect the memory to the information processor when the information processor and the gateway card are in the middle of booting.

3. The gateway card according to claim 1, wherein the memory is partitioned into a first partition corresponding to the information processor and a second partition corresponding to the gateway card, the gateway card further comprising a valid-invalid unit that

validates the first partition and invalidates the second partition when the information processor is in the normal power mode, and

invalidates the first partition and validates the second partition when the normal power mode is changed to the power saving mode.

4. The gateway card according to claim 1, further comprising a deciding unit that decides whether a data transfer speed of the information processor is different from that of the gateway card and whether the normal power mode is changed to the power saving mode, wherein

the switch control unit controls the switching unit to connect the memory to the gateway card, and initializes the memory so as to match the data transfer speed of the information processor with that of the gateway card, when it is decided that the data transfer speed of the information processor is different from that of the gateway card and that the normal power mode is changed to the power saving mode.

5. The gateway card according to claim 1, further comprising:

an access control unit that controls an access to the memory to allocate the access to the memory via the switching unit when the information processor is in the power saving mode, and allocate the access to the memory via the information processor and the switching unit when the power saving mode is returned to the normal power mode.

6. The gateway card according to claim 5, wherein

when switching of the switching unit occurs in the middle of the

access, the access control unit controls the access to be made to the memory once more after the switching is completed.

7. The gateway card according to claim 5, further comprising a swap out memory into which data is swapped out when data writing error occurs in the middle of the access.

8. The gateway card according to claim 5, further comprising a swap out memory, wherein

when data writing error occurs in the middle of the access, the access control unit swaps out data into the memory, and

when switching of the switching unit occurs during the swapping, the access control unit swaps out the data into the swap out memory, and merges the data swapped out to the memory with the data swapped out to the swap out memory.

9. The gateway card according to claim 5, further comprising a swap out memory, wherein

when data writing error occurs in the middle of the access, the access control unit swaps out data into the memory and the swap out memory, and

when switching of the switching unit occurs during the swapping, the access control unit merges the data swapped out to the memory with the data swapped out to the swap out memory.

10. A gateway device comprising:

a memory;

an information processor with a power control unit that shifts an operation status of the information processor from a normal power mode to a power saving mode and vice versa based on a predetermined condition; and

a gateway card that is connected to the information processor and that receives and transmits data between different networks, the gateway card including

a switching unit that connects the memory with either the information processor or the gateway card; and

a switch control unit that controls the switching unit to connect the memory to the information processor when the information processor is in the normal power mode, and controls the switching unit to connect the memory to the gateway card when the normal power mode of the information processor is changed to the power saving mode.

11. The gateway device according to claim 10, wherein

the switch control unit controls the switching unit to connect the memory to the information processor when the information processor and the gateway card are in the middle of booting.

12. The gateway device according to claim 10, wherein the memory has a first partition corresponding to the information processor and a

second partition corresponding to the gateway card, the gateway card further comprising a valid-invalid unit that

validates the first partition and invalidates the second partition when the information processor is in the normal power mode, and

invalidates the first partition and validates the second partition when the normal power mode is changed to the power saving mode.

13. The gateway device according to claim 10, wherein the gateway card further comprising a deciding unit that decides whether a data transfer speed of the information processor is different from that of the gateway card and whether the normal power mode is changed to the power saving mode, wherein

the switch control unit controls the switching unit to connect the memory to the gateway card, and initializes the memory so that the data transfer speed of the information processor is same as that of the gateway card, when it is decided that the data transfer speed of the information processor is different from that of the gateway card and that the normal power mode is changed to the power saving mode.

14. The gateway device according to claim 10, wherein the gateway card further comprising an access control unit that controls an access to the memory to allocate the access to the memory via the switching unit when the information processor is in the power saving mode, and allocate the access to the memory via the information processor and the switching unit when the power saving mode is returned to the

normal power mode.

15. The gateway device according to claim 14, wherein

the access control unit controls the access to be made to the memory once more after the switching is completed when switching of the switching unit occurs in the middle of the access.

16. The gateway device according to claim 14, wherein the gateway card further comprising a swap out memory into which the access unit swaps out data when data writing error occurs in the middle of the access.

17. The gateway device according to claim 14, wherein the gateway card further comprising a swap out memory, and

when data writing error occurs in the middle of the access, the access control unit swaps out data into the memory, and

when switching of the switching unit occurs during the swapping, the access control unit swaps out the data into the swap out memory, and merges the data swapped out to the memory with the data swapped out to the swap out memory.

18. The gateway device according to claim 14, wherein the gateway card further comprising a swap out memory, and

when data writing error occurs in the middle of the access, the access control unit swaps out data into the memory and the swap out

memory, and

when switching of the switching unit occurs during the swapping, the access control unit merges the data swapped out to the memory with the data swapped out to the swap out memory.

19. A method of controlling a gateway card, which is connected to an information processor and which receives and transmits data between different networks, the information processor having a normal power mode and a power saving mode, the method comprising:

connecting the information processor to a memory when the information processor is in the normal power mode; and

connecting the gateway card to the memory when the normal power mode of the information processor is changed to the power saving mode.

20. The method according to claim 19, further comprising connecting the information processor to the memory when the information processor and the gateway card are in the middle of booting.

21. The method according to claim 19, wherein the memory having a first partition corresponding to the information processor and a second partition corresponding to the gateway card, the method further comprising:

validating the first partition and invalidating the second partition

when the information processor is in the normal power mode; and

invalidating the first partition and validating the second partition when the normal power mode is changed to the power saving mode.

22. The method according to claim 19, further comprising:

deciding whether a data transfer speed of the information processor is different from that of the gateway card and whether the normal power mode is changed to the power saving mode; and

connecting the gateway card to the memory, and initializing the memory so as to match the data transfer speed of the information processor with that of the gateway card, when it is decided that the data transfer speed of the information processor is different from that of the gateway card and that the normal power mode is changed to the power saving mode.

23. The method according to claim 19, further comprising controlling access to the memory to allocate the access to the memory when the information processor is in the power saving mode and allocate the access to the memory via the information processor when the normal power mode is changed to the power saving mode.

24. The method according to claim 23, wherein the controlling performed once more after the switching is completed when the connecting occurs in the middle of the access.

25. The method according to claim 23, further comprising swapping out of data into a swap out memory when data writing error occurs in the middle of the access.

26. The method according to claim 23, further comprising:

swapping out of data into the memory when data writing error occurs in the middle of the access; and

swapping out of the data into a swap out memory when the connecting occurs during the swapping out of data into the memory, and merging the data swapped out to the memory with the data swapped out to the swap out memory.

27. The method according to claim 23, further comprising:

swapping out of data into the memory and a swap out memory when data writing error occurs in the middle of the access; and

merging the data swapped out to the memory with the data swapped out to the swap out memory when the connecting occurs during the swapping.

28. A method of controlling a gateway device having a memory; an information processor with a normal power mode and a power saving mode, wherein the normal power mode is changed to the power saving mode and vice versa based on a predetermined condition; and a gateway card that is connected to the information processor and that receives and transmits data between different networks, the method

comprising:

connecting the information processor to the memory when the information processor is in the normal power mode; and

connecting the gateway card to the memory when the normal power mode of the information processor is changed to the power saving mode.

29. The method according to claim 28, further comprising connecting the information processor to the memory when the information processor and the gateway card are in the middle of booting.

30. The method according to claim 28, wherein the memory has a first partition corresponding to the information processor and a second partition corresponding to the gateway card, the method further comprising

validating the first partition and invalidating the second partition when the information processor is in the normal power mode; and

invalidating the first partition and validating the second partition when the normal power mode is changed to the power saving mode.

31. The method according to claim 28, further comprising

deciding whether a data transfer speed of the information processor is different from that of the gateway card and whether the normal power mode is changed to the power saving mode; and

connecting the gateway card to the memory, and initializing the memory so as to match the data transfer speed of the information processor with that of the gateway card when it is decided that the data transfer speed of the information processor is different from that of the gateway card and that the normal power mode is changed to the power saving mode.

32. A computer program that realizes on a computer a method for controlling a gateway card, which is connected to an information processor and which receives and transmits data between different networks, the information processor having a normal power mode and a power saving mode, the computer program making the computer execute:

connecting the information processor to a memory when the information processor is in the normal power mode; and

connecting the gateway card to the memory when the normal power mode of the information processor is changed to the power saving mode.

33. A computer program that realizes on a computer a method of controlling a gateway device having a memory; an information processor with a normal power mode and a power saving mode, wherein the normal power mode is changed to the power saving mode and vice versa based on a predetermined condition; and a gateway card that is connected to the information processor and that receives

and transmits data between different networks, the computer program making the computer execute:

connecting the information processor to the memory when the information processor is in the normal power mode; and

connecting the gateway card to the memory when the normal power mode of the information processor is changed to the power saving mode.